

What is claimed is:

1. A differential amplifier comprising:
a differential amplifier circuit comprising
first and second differential amplifier sections;
5 wherein said first differential amplifier
section comprises:
a first differential pair of PMOS transistors
which receives first and second input voltages,
respectively;
10 wherein said second differential amplifier
section comprises:
a second differential pair of NMOS
transistors which receive said first and second input
voltages, respectively;
15 a bias circuit which activates one of said
first and second differential amplifier sections in
response to a control signal; and
an output circuit which outputs an output
signal from an output of said activated differential
20 amplifier section.

2. The differential amplifier according to claim
1, wherein said first and second differential
amplifier sections comprise a first PMOS transistor
25 and a first NMOS transistor function as constant
current sources, respectively,
said bias circuit stops an operation of said

first PMOS transistor when activating said second differential amplifier section, and stops an operation of said first NMOS transistor when activating said first differential amplifier section.

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3. The differential amplifier according to claim 2, wherein said bias circuit comprises:

a first switch arranged to connect a first bias voltage to a gate of said first PMOS transistor
10 in response to said control signal; and

a second switch arranged to connect a second bias voltage to a gate of said first NMOS transistor in response to said control signal, and

when one of said first and second switches is
15 turned on, the other is turned off.

4. The differential amplifier according to claim 3, wherein said bias circuit comprises:

an inverter which inverts said control
20 signal;

a third switch which is connected between said power supply line and the gate of said first PMOS transistor and switches in response to the inverted control signal; and

25 a fourth switch which is connected between said ground line and the gate of said first NMOS transistor and switches in response to the inverted

control signal,

when one of said third and fourth switches is turned on, the other is turned off.

5 5. The differential amplifier according to claim 4, wherein when said first switch is turned on, said third switch is turned off, and when said second switch is turned on, said fourth switch is turned off.

10 6. The differential amplifier according to claim 1, wherein said first differential amplifier section comprises:

a first current mirror circuit whose input is connected with an output from one of said PMOS transistors of said first differential pair; and

a second current mirror circuit whose input is connected with an output from the other of said PMOS transistors of said first differential pair, said second differential amplifier section

20 comprises:

a third current mirror circuit, one of whose outputs is connected with an input of one of said NMOS transistors of said second differential pair; and

a fourth current mirror circuit, one of whose outputs is connected with an input of the other of said NMOS transistors of said second differential pair.

7. The differential amplifier according to claim 6, wherein the other output of said third current mirror circuit is connected with the input of said second current mirror circuit, and

5 the other output of said fourth current mirror circuit is connected with the input of said first current mirror circuit.

8. The differential amplifier according to claim 10 7, wherein said output circuit obtains the output of said activated differential amplifier section from said third and fourth current mirror circuits.

9. The differential amplifier according to claim 15 1, further comprising:

a control signal generating circuit which generates said control signal based on said first and second input voltages.

20 10. The differential amplifier according to claim 9, wherein said control signal generating circuit comprises:

a first circuit which generates an average voltage of said first and second input voltages; and

25 a second circuit which generates said control signal from said average voltage.

11. The differential amplifier according to claim
10, wherein said first circuit comprises:

a second constant current source connected
with said ground line;

5 third NMOS transistors which are connected
with said second constant current source and receives
said first and second input voltages at gates of said
third NMOS transistors;

fourth NMOS transistors which are connected
10 with said second constant current source; and

a current mirror which is connected with said
power supply line and supplies said fourth NMOS
transistor with a current equal to a sum of currents
flowing through said third NMOS transistors, and

15 said average voltage is outputted from a node
between said current mirror and said fourth NMOS
transistors.

12. The differential amplifier according to claim
20 11, wherein said second circuit comprises:

a comparator which compares a predetermined
reference voltage and said average voltage to output
said control signal.

25 13. The differential amplifier according to claim
11, wherein said control signal generating circuit
further comprises:

a filter circuit which is provided between
said first and second circuits.

14. The differential amplifier according to claim
5 11, wherein said first circuit further comprises:

a buffer which is connected between said node
and said second circuit.

15. A method of outputting an output signal from
10 first and second input voltages in an differential
amplifier circuit comprising first and second
differential amplifier sections, wherein said first
differential amplifier section comprises a first
differential pair of PMOS transistors which
15 respectively receives first and second input voltages,
and wherein said second differential amplifier section
comprises a second differential pair of NMOS
transistors which respectively receives said first and
second input voltages, said method comprising:

20 activating one of said first and second
differential amplifier sections in response to a
control signal;

supplying first and second input voltages to
said activated differential amplifier section; and

25 outputting an output signal from an output of
said activated differential amplifier section.

16. The method according to claim 15, wherein said activating comprises:

(a) controlling a first constant current source for said first differential amplifier section to be tuned on and a second constant current source for said second differential amplifier section to be turned off when said first differential amplifier section is activated in response to said control signal; and

(b) controlling said second constant current source to be turned on and said first constant current source to be turned off when said second differential amplifier section is activated in response to said control signal.

17. The method according to claim 16, wherein said (a) controlling comprises:

supplying a first bias voltage to a gate of a first PMOS transistor of said first constant current source; and

stopping the supply of said first bias voltage to the gate of said first PMOS transistor.

18. The method according to claim 16, wherein said (b) controlling comprises:

supplying a second bias voltage to a gate of a first NMOS transistor of said second constant

current source; and

stopping the supply of said second bias voltage to the gate of said first NMOS transistor.

5 19. The method according to claim 16, wherein said activating comprises:

inverting said control signal;

stopping an operation of said second constant current source in response to the inverted control
10 signal, when said first differential amplifier section is activated in response to said control signal; and

stopping an operation of said first constant current source in response to the inverted control signal, when said second differential amplifier
15 section is activated in response to said control signal.

20. The method according to claim 15, further comprising:

20 generating said control signal based on said first and second input voltages.